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**SECOND SEMESTER 2023-2024**

# Course Handout Part II

Date: 09-01-2024

In addition to part-I (General Handout for all courses appended to the time table) this portion gives further specific details regarding the course.

*Course No.* : CS/ECE/EEE/INSTR F241

## Course Title : Microprocessor Programming and Interface

## Instructor-in-Charge : Dr. Subhradeep Pal

*Team of Instructors* : Dr. Anakhi Hazarika, Prof. Runa Kumari, Prof. Soumya J, Dr. Sourav Nandi

**Scope and Objective of the Course:**

The objective of this course is to become familiar with the processor internal architecture and its operation within the area of manufacturing and performance. This course will provide the instruction set of an Intel microprocessor 8086 – 80486, programmers model of processor, demonstration of the modular assembly programming using the various addressing modes, data transfer instructions, subroutines, macros etc.; Timing diagrams; Concept of interrupts: hardware & software interrupts, Interrupt handling techniques, Interrupt controllers; Types of Memory & memory interfacing; Programmable Peripheral devices and I/O Interfacing; DMA controller and its interfacing: Design of processor based system. This course familiarizes the students with the programming and interfacing of microprocessors, which will help in solving basic binary math operations using the microprocessor and provide a strong foundation for designing real world applications using microprocessors.

**Textbooks:**

1. **T1**: Barry B. Brey, The Intel Microprocessors: Architecture, Programming and Interfacing, Pearson, 8th Edition, 2009.

**Reference books**

1. **R1:** D. V. Hall, Microprocessor and Interfacing, Tata McGraw Hill, 2nd Edition.
2. **R2:** L. B. Das, The x86 Microprocessors, 2nd Edition, Pearson.
3. **R3:** N. Senthil Kumar, M. Saravanan, and S. Jeevanathan, Microprocessors and Microcontrollers,

Oxford University Press.

**Course Plan:**

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| **Lec. No.** | **Learning objectives** | **Topics to be covered** | **Chapter in the Text Book** |
| 1-2 | Introduction to microprocessor and microcomputers | Introduction to microprocessors, Historical background, Basics of computer architecture, Memory & I/O organization, CISC, RISC, EPIC Processors and Flynn’s Taxonomy | T1: Chap. 1  R1: Chap. 1 |
| 3-4 | Architecture of 8086 | Detailed architecture of 8086, Pin configurations of 8086, Modes of Operation, Clocking and Buses | T1: Chap. 2 and 9  R1: Chap. 2 |
| 5-6 | Assembly Language Programming: Part I | Addressing Modes | T1: Chap. 3 |
| 7-10 | Assembly Language Programming: Part II | Instruction set of 8086: Data transfer, logical, arithmetic, flag manipulation, control transfer, rotate, string, processor control instructions. | T1: Chap. 4-8  R3: Chap. 13 |
| 11-13 | Assembly Language Programming: Part III | ALP Examples and practical examples of usage of 8086 | T1: Chap. 4-8  R3: Chap. 14 |
| 14-15 | Interrupts | Types of 8086 interrupts, vector table, priority among 8086 interrupts, interrupt service routine, practical examples | T1: Chap. 12  R3: Chap. 15 |
| 16-19 | Memory Interface | Physical Memory Organization of 8086, Memory Devices, Address Decoding, Memory Interface: Interfacing RAM and EPROM using logic gates/ decoder ICs. | T1: Chap. 10  R3: Chap.16 |
| 20-24 | I/O Interface | Basic I/O, I/O Instructions, I/O mapped and memory mapped I/O, Interfacing with 8-bit I/O devices, I/O port address decoding | T1: Chap. 11  R3: Chap. 16 |
| 25-28 | Programmable Peripheral Devices | 8255: General purpose PPI  8254: Programmable Interval Controller  8259: Programmable Interrupt Controller  ADCs and DACs | T1: Chap. 11  T1: Chap. 12 |
| 29-31 | DMA Controller | 8237: Basic Operation, Pin Details, Features, Architecture, DMA Initialization, Operation with 8086 | T1: Chap. 13  R3: Chap. 7 |
| 32-34 | Bus Interface | ISA, PCI, USB etc | T1: Chap. 15 |
| 35-37 | Advanced Processor Part I | 80186-80286 | T1: Chap. 16  R1: Chap. 15 |
| 38-40 | Advanced Processor Part II | 80386 and 80486 | T1: Chap. 17  R1: Chap 15 |
| 41-42 | Coprocessor for x86 family | 8087: Pin layout, Architecture, Registers, Interfacing with 8086, Instruction Set, Application examples | Lecture Notes/Slides |

**Evaluation Scheme:**

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| **Sl. No.** | **Component** | **Duration** | **Weightage (%)** | **Marks** | **Date & Time** | **Nature of Component** |
| 1. | Mid-Term Examination | 90 mins. | 30% | 90 | 11/03 - 2.00 - 3.30PM | Closed Book |
| 2. | 3 Announced Quizzes with (n-1) scheme | 30 mins. Each | 10% | 30 | TBA | Closed Book |
| 3. | Regular Lab Evaluations with (n-1) scheme | 120 mins. / week | 17% | 50 | As per timetable | Open Book |
| 4. | Comprehensive Lab Exam Quiz Test | 30 mins | 3% | 10 | TBA | Open Book |
| 5. | Comprehensive Examination | 3 hours | 40% | 180 | 07/05 FN | Closed Book |

**Chamber Consultation Hour:** This will be announced in the class.

**Notices:** All notices will be displayed via CMS only.

**Make-up Policy:**

1. **Both announced quizzes and regular lab evaluations will strictly follow the (n-1) scheme.**
2. **The course will follow a zero-make-up policy for the announced quizzes and regular lab evaluations.**
3. **Makeup will be allowed for mid-term and end-term examinations only on the basis of genuine medical grounds with prior intimation and proper submission of correct and necessary documents.**

**Academic Honesty and Integrity Policy:**

Academic honesty and integrity are to be maintained by all the students throughout the semester; no academic dishonesty is acceptable.

**INSTRUCTOR-IN-CHARGE**